UMC

T-46-23-12

UM6116-2/-3 Series

2K× 8 CMOS SRAM

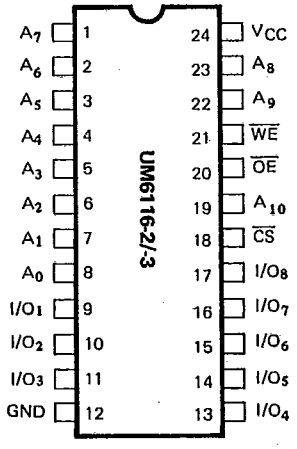
Features

- Single +5 volt power supply
- Access times: 90/120 ns (max.)
- Current:
  - for UM6116-3/-3T Operating: 100 mA (max.)
    Standby: 100 μA (max.)
  - for UM6116-2/-2T Operating: 100 mA (max.)
    Standby: 50 μA (max.)
  - for UM6116-3L/-2L/-3LT/-2LT
    Operating: 50 mA (max.)
    Standby: 1 μA (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output
- Pin compatible with standard 16K EPROM/Mask ROM
- UM6116-2/-3 is the standard version of UM6116-2/-3 series
- UM6116-2L/-3L is the low power version of UM6116-2/-3 series
- UM6116-2T/-3T is the wide temperature version of UM6116-2/-3 series
- UM6116-2LT/-3LT is the low power, wide temperature version of UM6116-2/-3 series
- Available in 24 pin DIP, SOP, or Skinny DIP packages (See ordering information)

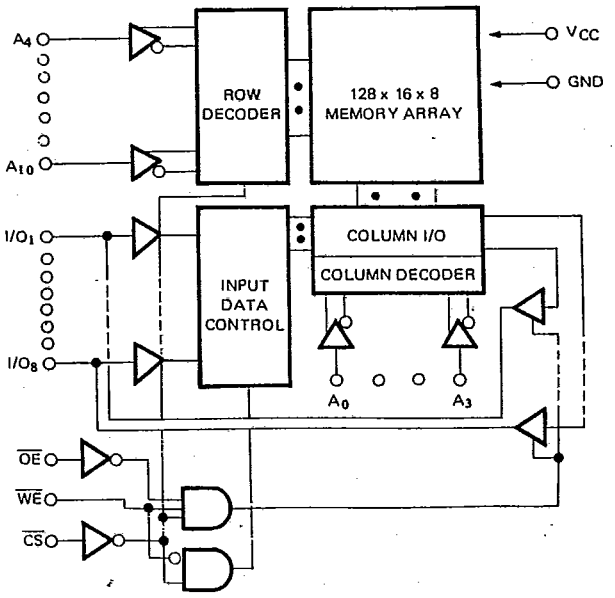
General Description

The UM6116-2/-3 series is a 16,384-bit static random access memory organized as 2,048 words by 8 bits and operates on a single 5-volt supply. It is built with UMC's high performance CMOS process. Six-transistor full CMOS memory cell provides low standby current and high reliability. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Pin Configuration



Block Diagram



Pin Description

Designation	Description
$A_0 - A_{10}$	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
$I/O_1 - I/O_8$	Data Input/Output
V_{CC}	Power Supply (+5V)
GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to 70°C for UM6116-2/-3, UM6116-2L/-3L
T_A = −40°C to 85°C for UM6116-2T/-3T, UM6116-2LT/3LT)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	V_{CC}+ 0.5V	V
V_{IL}	Input Low Voltage	−0.3	0	0.8	V
C_L	Output Load	–	–	100	pF
TTL	Output Load	–	–	1	–

Absolute Maximum Ratings *

V_{CC} to GND ..... −0.5V to +7.0V
IN, IN/OUT Volt to GND ..... −0.5V to V_{CC} +0.5V
Operating Temperature, T_{opr} ... 0°C to +70°C (Note 1)
Storage Temperature, T_{stg} ..... −55°C to +125°C
Temperature Under Bias, T_{bias} ... −10°C to +85°C (Note 1)
Power Dissipation, P_T 1.0W/SOP 0.7W
Soldering temp. & time ..... 260°C, 10 sec

Note 1: for UM6116-2T/-3T, UM6116-2LT/-3LT
T_{opr}: −40°C to 85°C , T_{bias}: −50°C to 95°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, GND = 0V, T_A = −40°C to 85°C for T version)

Symbol	Item	UM6116-3/ UM6116-3T		UM6116-2/ UM6116-2T		UM6116-3L/ UM6116-2L, UM6116-3LT/ UM6116-2LT		Unit	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current	–	10	–	10	–	1	μA	V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current	–	10	–	10	–	1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = GND to V_{CC}
I_{CC}	Active Power Supply Current	–	100	–	100	–	50	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
I_{CC1}	Dynamic Operating Current	–	100	–	100	–	50	mA	Min. Cycle, duty = 100%, $\overline{CS}$ = V_{IL} $I_{I/O}$ = 0 mA
I_{SB}	Standby Power Supply Current	–	1	–	1	–	1	mA	$\overline{CS}$ = V_{IH}
I_{SB1}		–	100	–	50	–	1	μA	$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	–	0.4	–	0.4	–	0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4	–	2.4	–	2.4	–	V	I_{OH} = −1.0 mA

Truth Table

Mode*	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}, I_{SB1}
Output Disabled	L	H	H	High Z	I_{CC}, I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC}, I_{CC1}
Write	L	X	L	D_{IN}	I_{CC}, I_{CC1}

Note: X:H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

*This parameter is sampled and not 100% tested.

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AC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, for UM6116-2/-3, UM6116-2L/-3L
T_A = −40°C to 85°C for UM6116-2T/-3T, UM6116-2LT/-3LT)

Symbol	Parameter	UM6116-3/-3L/ UM6116-3T/ UM6116-3LT		UM6116-2/-2L/ UM6116-2T/ UM6116-2LT		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	90	–	120	–	ns
t_{AA}	Address Access Time	–	90	–	120	ns
t_{ACS}	Chip Select Access Time	–	90	–	120	ns
t_{OE}	Output Enable to Output Valid	–	50	–	50	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	–	10	–	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	10	–	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	40	0	40	ns
t_{OHZ}	Output Disable to Output in High Z	0	40	0	40	ns
t_{OH}	Output Hold from Address Change	5	–	10	–	ns
WRITE CYCLE						
t_{WC}	Write Cycle Time	90	–	120	–	ns
t_{CW}	Chip Selection to End of Write	55	–	70	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	ns
t_{AW}	Address Valid to End of Write	80	–	85	–	ns
t_{WP}	Write Pulse Width	55	–	70	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High Z	0	40	0	40	ns

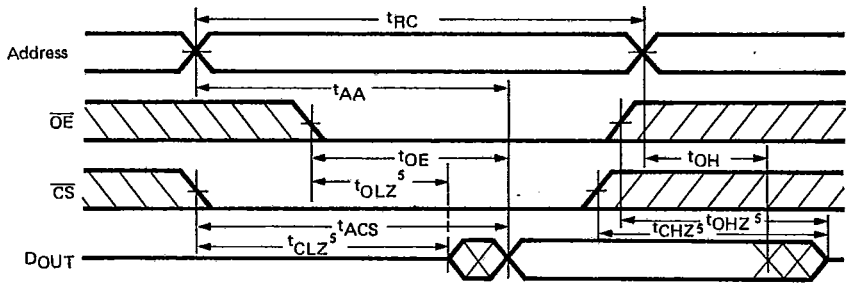
AC Electrical Characteristics (Continued)

Symbol	Parameter	UM6116-3/-3L UM6116-3T/ UM6116-3LT		UM6116-2/-2L UM6116-2T/ UM6116-2LT		Unit
		Min.	Max.	Min.	Max.	
t_{WHZ}	Write to Output in High Z	0	50	0	50	ns
t_{DW}	Data to Write Time Overlap	30	–	35	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	ns
t_{OW}	Output Active from End of Write	0	–	5	–	ns

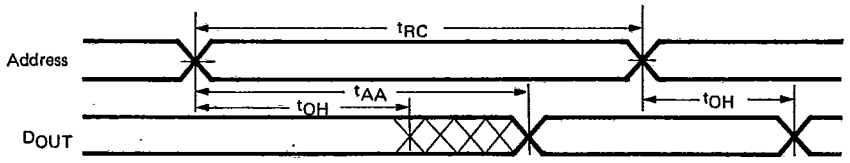
Notes: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

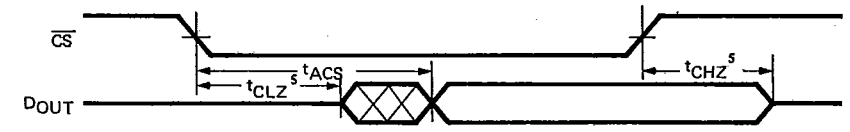
READ CYCLE 1 (1)



READ CYCLE 2 (1, 2, 4)

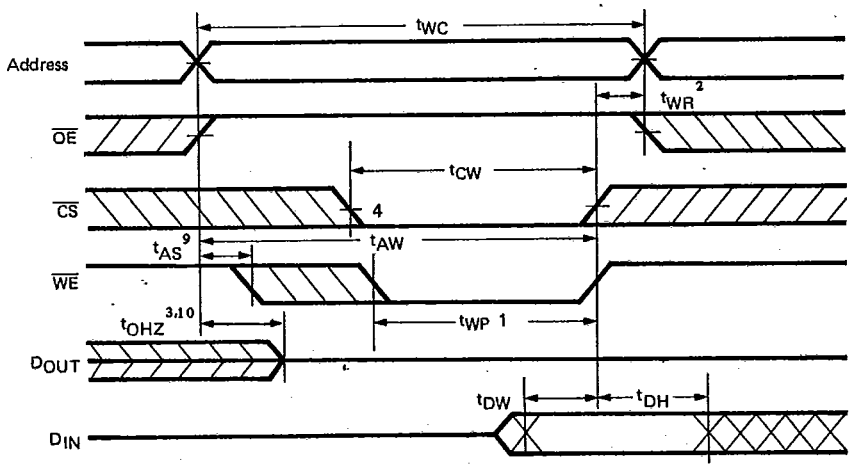


READ CYCLE 3 (1, 3, 4)

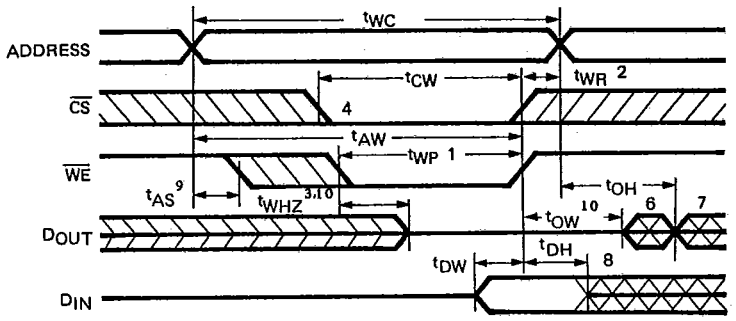


Notes:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±500mv from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2 (5)

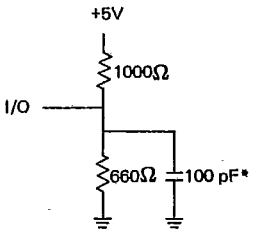


Notes:

1. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
6. D_{OUT} is the same phase of write data in this write cycle.
7. D_{OUT} is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. t_{AS} is measured from the address valid to the beginning of write.
10. Transition is measured ±500 mV from steady state, this parameter is sampled and not 100% tested.

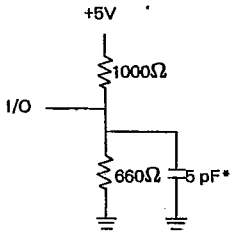
AC Test Conditions

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 2



*Including scope and jig.

Figure 1. Output Load



*Including scope and jig.

Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

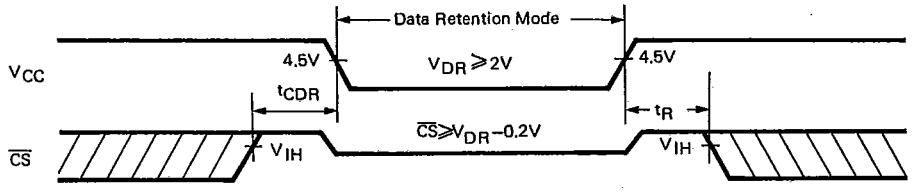
Data Retention Characteristics

L versions only (T_A = 0°C to +70°C for UM6116-2L/UM6116-3L
T_A = −40°C to +85°C for UM6116-2LT/UM6116-3LT)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DR}	V_{CC} for Data Retention	2.0	—	V	$\overline{CS} \geq V_{CC}-0.2V$
I_{CCDR}	Data Retention Current	—	20	μA	V_{CC} = 3.0V, $\overline{CS} \geq V_{CC}-0.2V$
t_{CDR}	Chip Deselect to Data Retention Time	0	—	ns	See Retention
t_R	Operation Recovery Time	t_{RC}*	—	ns	Waveform

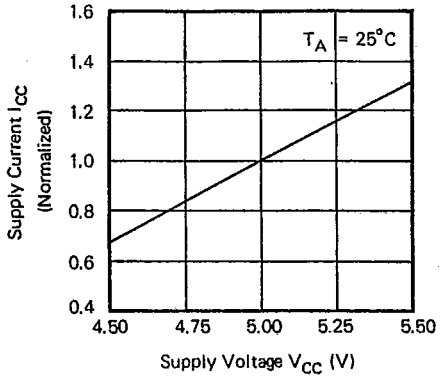
*t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform

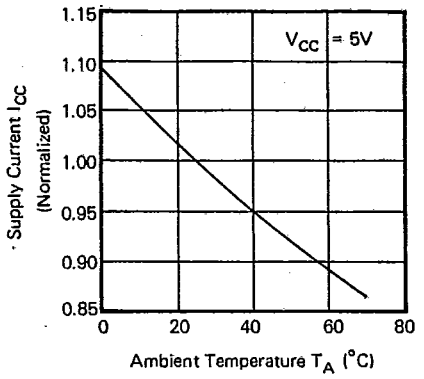


Characteristic Curves

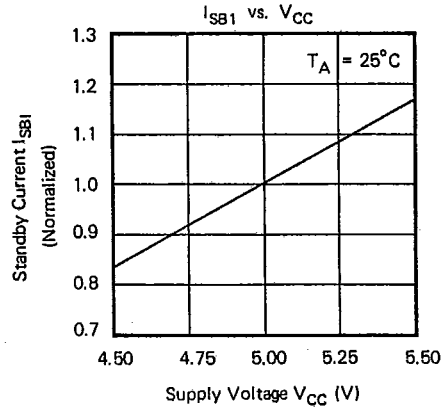
I_{CC} vs. V_{CC}



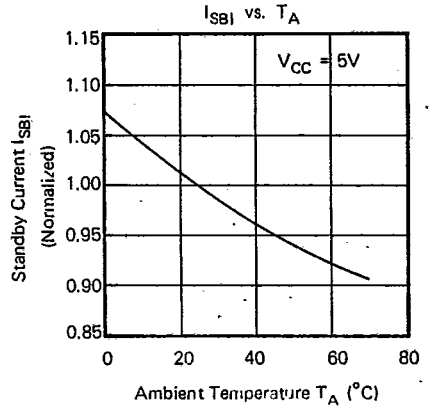
I_{CC} vs. T_A



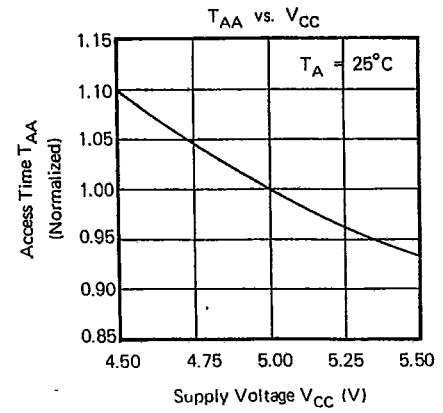
I_{SB1} vs. V_{CC}



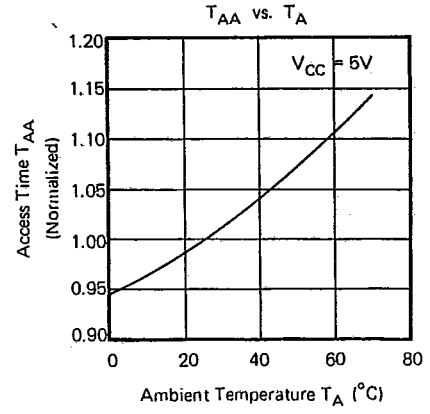
I_{SB1} vs. T_A



T_{AA} vs. V_{CC}



T_{AA} vs. T_A



Standard SRAM

Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Temperature Range	Package
UM6116-2	120 ns	100	0.05	0°C to 70°C	24L DIP
UM6116-3	90 ns	100	0.1		24L DIP
UM6116M-2	120 ns	100	0.05	0°C to 70°C	24L SOP
UM6116M-3	90 ns	100	0.1		24L SOP
UM6116K-2	120 ns	100	0.05	0°C to 70°C	24L Skinny DIP
UM6116K-3	90 ns	100	0.1		24L Skinny DIP
UM6116-2T	120 ns	100	0.05	−40°C to 85°C	24L DIP
UM6116-3T	90 ns	100	0.1		24L DIP
UM6116M-2T	120 ns	100	0.05	−40°C to 85°C	24L SOP
UM6116M-3T	90 ns	100	0.1		24L SOP
UM6116K-2T	120 ns	100	0.05	−40°C to 85°C	24L Skinny DIP
UM6116K-3T	90 ns	100	0.1		24L Skinny DIP
UM6116-2L	120 ns	50	0.001	0°C to 70°C	24L DIP
UM6116-3L	90 ns	50	0.001		24L DIP
UM6116M-2L	120 ns	50	0.001	0°C to 70°C	24L SOP
UM6116M-3L	90 ns	50	0.001		24L SOP
UM6116K-2L	120 ns	50	0.001	0°C to 70°C	24L Skinny DIP
UM6116K-3L	90 ns	50	0.001		24L Skinny DIP
UM6116-2LT	120 ns	50	0.001	−40°C to 85°C	24L DIP
UM6116-3LT	90 ns	50	0.001		24L DIP
UM6116M-2LT	120 ns	50	0.001	−40°C to 85°C	24L SOP
UM6116M-3LT	90 ns	50	0.001		24L SOP
UM6116K-2LT	120 ns	50	0.001	−40°C to 85°C	24L Skinny DIP
UM6116K-3LT	90 ns	50	0.001		24L Skinny DIP